U.S. Appln. No. Unknown Attorney Docket, No. A7914

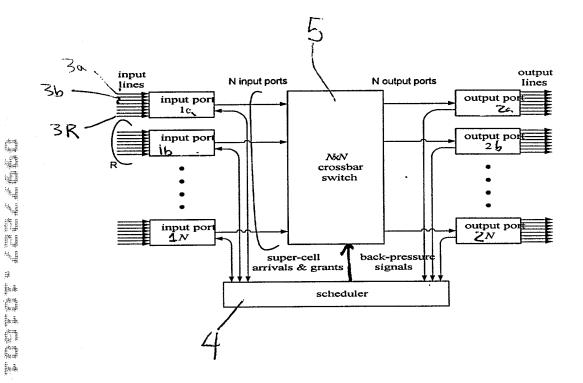


FIGURE I

paramete	meaning	typical value
N	number of input and output po	rts 64
L	number of input and output lin	
R	number of lines per port	8
K	number of classes	8
M	number of scheduling module	s 16
S	number of pipeline stages per scheduling module	1
C	number of cells per super-cell	8

FIGURE 2

U.S. Appln. No. Unknown Attorney Docket No. A7914

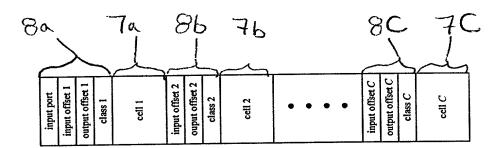


FIGURE 3

input port i

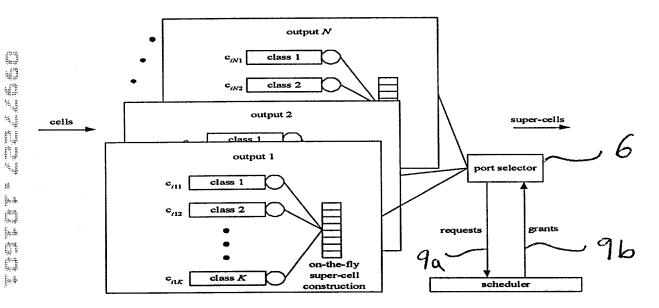
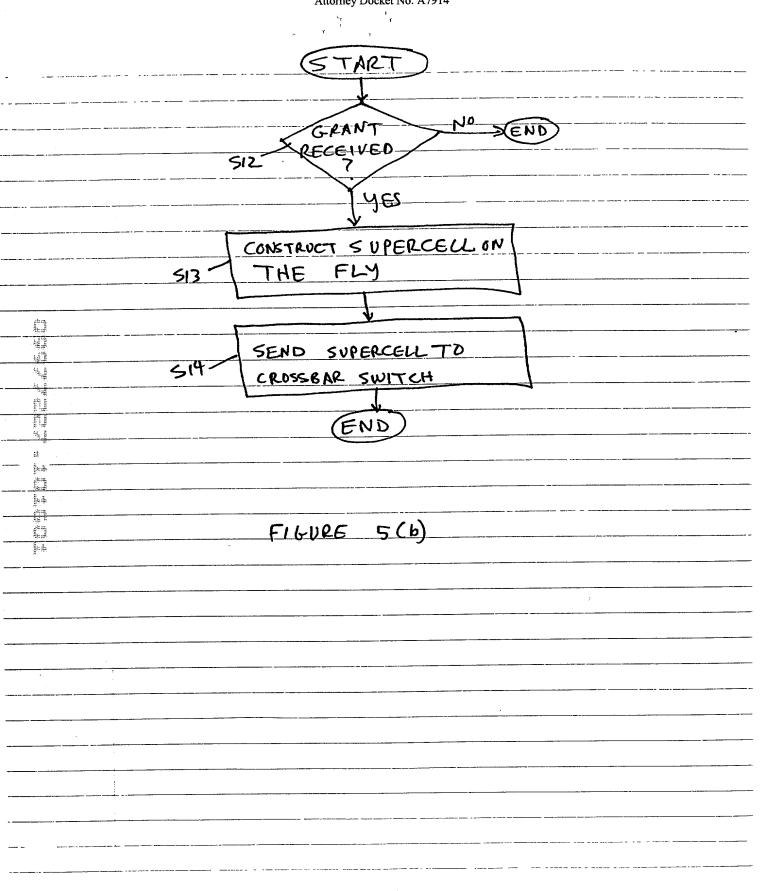
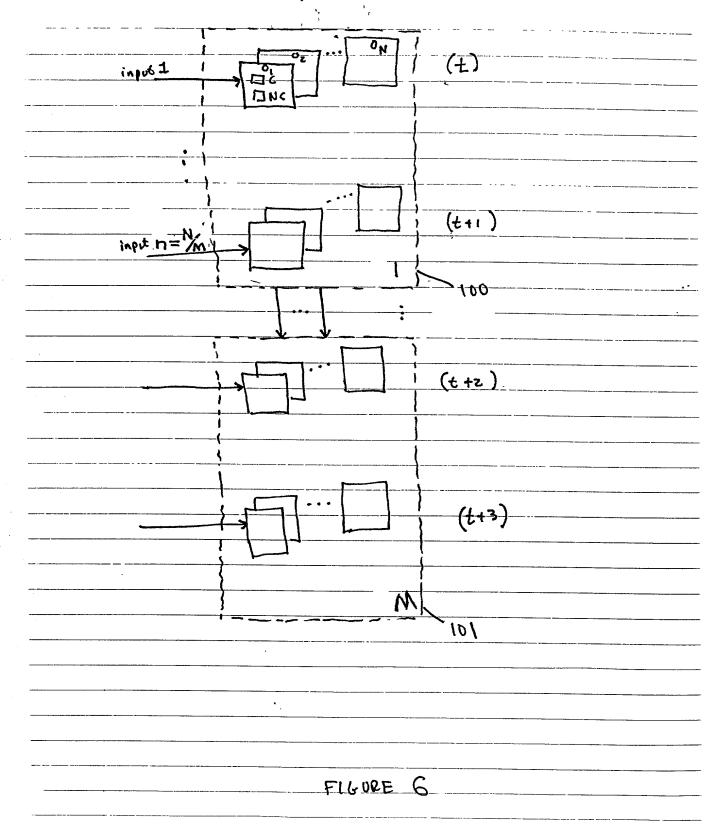


FIGURE 4

U.S. Appln. No. Unknown Attorney Docket No. A7914 START 5] PORT CELL ARRIVES INPUT AT BASED ON LOOK-UP TABLE CELL QUEUED 528 COUNTER FOR THE QUEUE UPDATE DREDIT CREDITS VAILABLE? INCREMENT NON-CONFORMING IN CREMENT CONFORMING CELL COUNTER CELL COUNTER W] 59 W. ENOUGH CELLS ENOUGH CELLS END for non-confirmation FOR CONFORMING SUPERCEUL? SUPERCELL T 56 A EZ y es 510 SEND REQUEST FOR SEND REQUEST FOR **L** CONFORMING SUPERCELL NON-CONFORMING SUPERCELL TO SCHEAULER SCHEDULER 44 DE CREMENT CONFORMING DECREMENT CINFORMING CELL COUNTER BY C COUNTER BY C 511 (END) 57 END FIGURE 5(a)





the transfer of the time that the that

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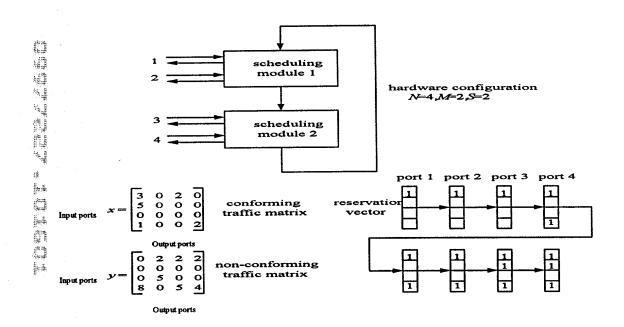


FIGURE 7

tioney Dock

module	-	n	ml			lay n			12		delay		m3			delay			m	4	4		ay	
stages	5	1	s 2				* 3		s 4					5	s 6				* 7		s 8			
ports		p2 p4							p13 p1 þ15 p1						ф21 p2 ф23 p2				p25 p2 p27 p2					
time slots		0	13	2	13	[3]	Į,	0	-	T.	3	•	3	0	20		23	•	2	<u></u>	23	<u> </u>	2	
	24	13	0	<u> </u>	13	2	13	•	14	0	1	<u>.</u>	3	•	ន្ទ	7	20	•	23	0	22	[-]	23	
+	23	0	2-	13	13	<u> </u>	13	2	13	3	19	0	1	4	[3	•	2	7	20	•	21	9	22	[19]
	22	[19	23	[]	24	12	13	0	1	2	13	3	13	0	17	3	3	9	3	0	200		21	0
	21	9	22	19	23	<u> </u>	24	12	13	0	13	2	13	3	14	0	•	9	13	0	[]	7	20	
	20	•	21	0	22	19	23	11	2	12	13	0	1	[2]	13	[•]	19	0	17	•		0	[2]	7
	9	Ø	20	[-]	21	0	22	10	23	0	24	12	13	0	13	[2]	13	0	13	0	17	3		•
		6	13	7	20	•	21	9	2	10	23	•	24	[2]	13	0	13	[2]	13	[]	14	0	17	3
	13	[]	19	0	19	7	20	6	21	9	22	19	23	[i]	24	12	13	0	13	2	13	0	19	•
	14	Ī		[]	19	6	13	7	29	0	21	0	22	19	23	<u> </u>	24	[3	13	0	13	2	13	•
	13	0	13	0	13	[3]	13	0	13	0	29	•	21	0	2	19	23	1	24	9	0	0	0	[2]
	Ī	[]	13	0	9	0	0	0	13	6	9	0	2	[23	0	2	[19	3	<u> </u>	2	13	13	0

FIGURE 8

	1 1
	START
	RECEIVE REQUEST FROM \$15
	INPUT BUFFER MODULE
	INCREMENT CONF. OR NON-CONF.
	COUNTER, DEPENDING ON REQUEST 516
	TYPE
then the had by Built Built	
* <u>*</u>	END
•	
· · · · · · · · · · · · · · · · · · ·	
	FIGURE 9

START SCHEDOLE SUPERCELL FOR CONNECTED INPUT, 517 FOR TRANSPORT AT A FUTURE TIME SLOT TRANSMIT GRANT TO CONNECTED INPUT 518 TRANSMIY RESERVATION STATUS TO NEXT CHIP/SM IN THE SCHEOULER 43 520 (END) FRAME ND i e Ű1 10 FIGURE

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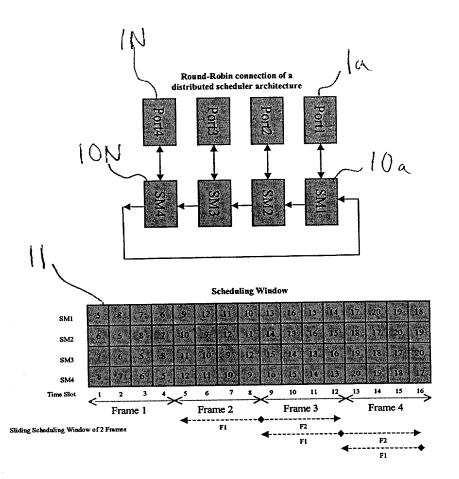
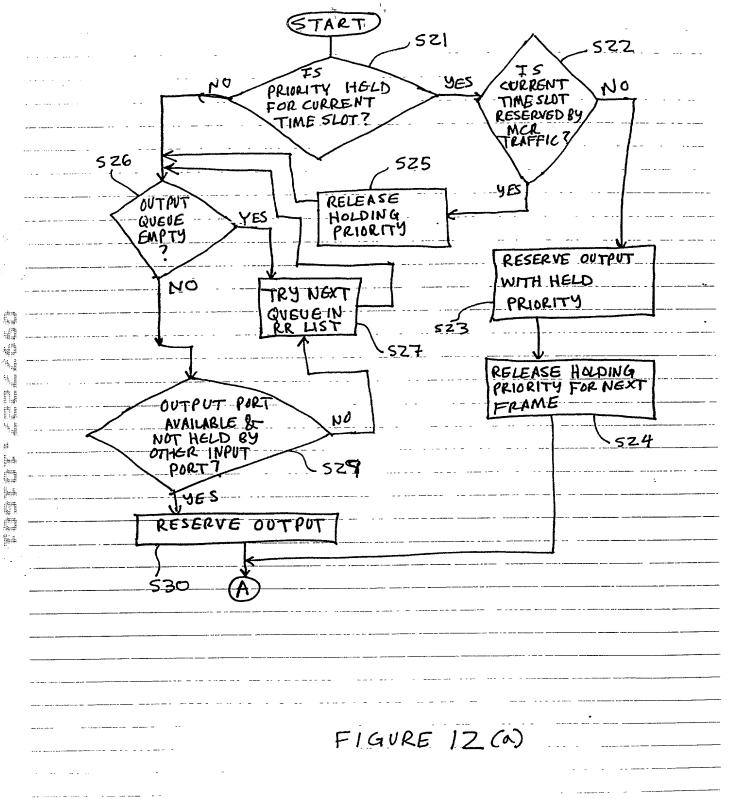


FIGURE . 11

The state of the s

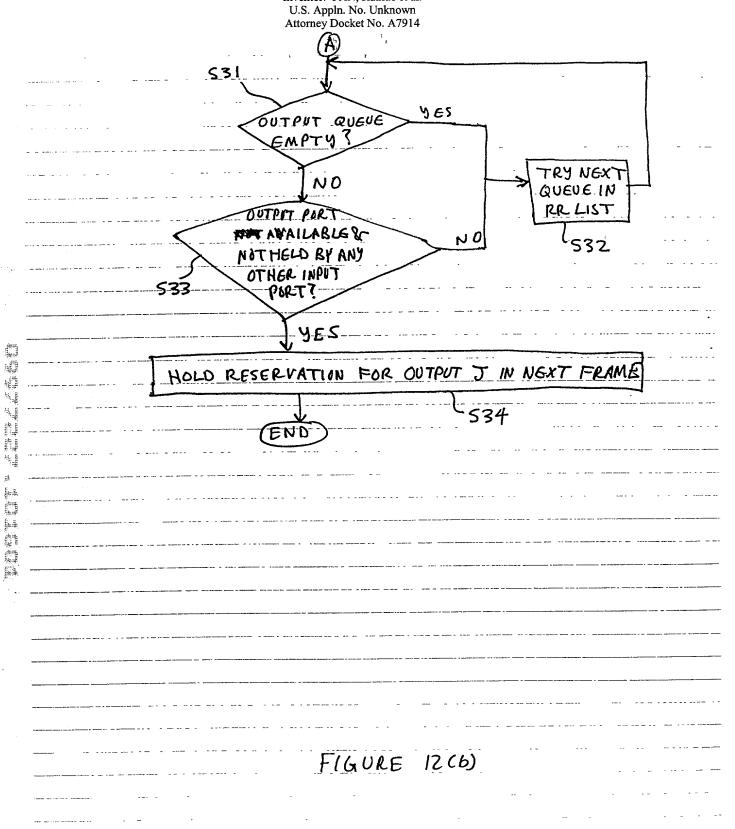
Title: Pipeline Scheduler With Fairness and Minimum Bandwidth Guarantee

Inventor: FAN, Ruixue et al. U.S. Appln. No. Unknown Attorney Docket No. A7914



43

Title: Pipeline Scheduler With Fairness and Minimum Bandwidth Guarantee Inventor: FAN, Ruixue et al.



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Title: Pipeline Scheduler With Fairness and Minimum Bandwidth Guarantee

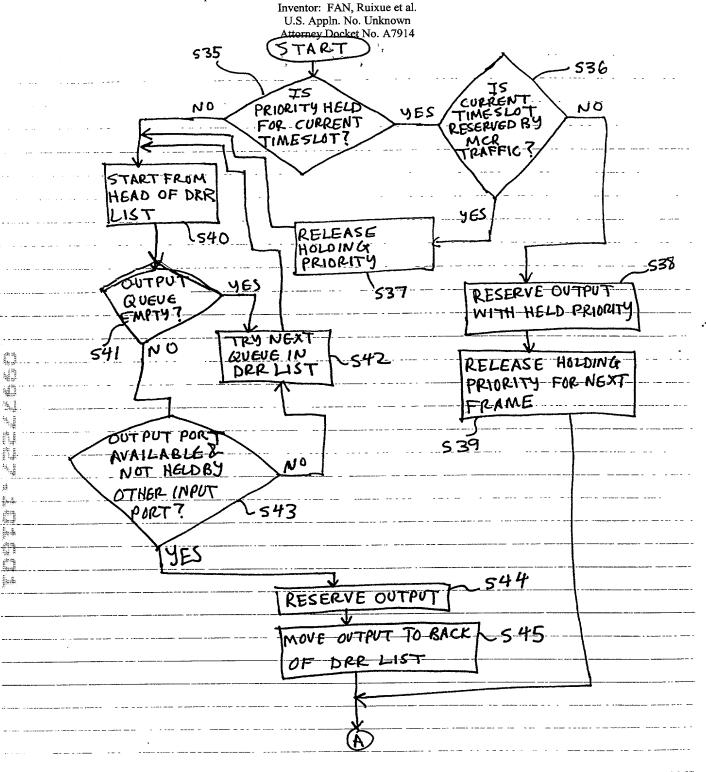
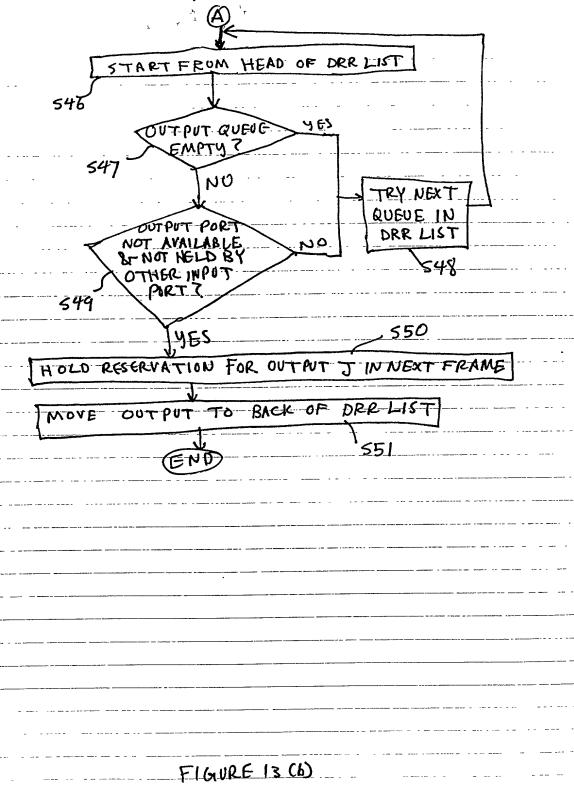


FIGURE 13(A)

Title: Pipeline Scheduler With Fairness and Minimum Bandwidth Guarantee

Inventor: FAN, Ruixue et al. U.S. Appln. No. Unknown Attorney Docket No. A7914



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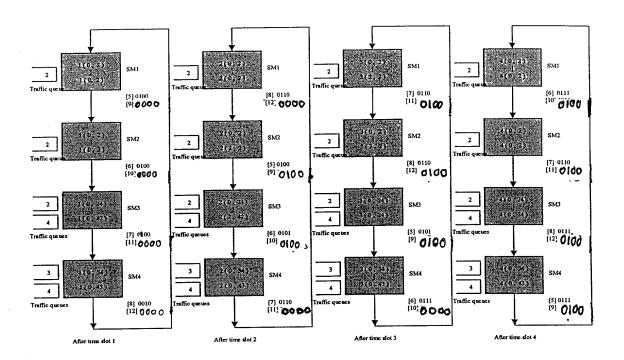


FIGURE 14 (a)

Inventor: FAN, Ruixue et al. U.S. Appln. No. Unknown Attorney Docket No. A7914

SMI 2 [10] 0101 [14] **0 1** 00 [11] 0111 [15] 000 [[12] 0001 [16 0 [0 0 [9] 0000 [13] **O10**0 SM2 SM2 SM2 SM2 [11] OLU ! [10] 0000 [14] **0] 00** [12] 0101 [16] **CIGO** [13] **OpeQ** [8] 0100 SM3 SM3 вмз SM3 [9] 0101 [13] **0 | 00** [12] 0101 [16] **0 (00** [10] 0100 [14] **0.000** [15] **010**0 SM4 [11] 00 11 [15] 01 0l [10] 0101 [14] **0000** [9] 0111 [13] **0]0**] [12] 0001 [16] **DIOO** After time slot 7 After time slot 5 After time slot 6

FIGURE 14(6)

U.S. Appln. No. Unknown Attorney Docket No. A7914

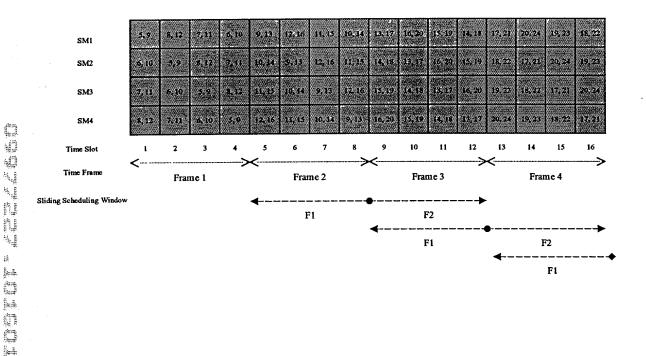


FIGURE 15

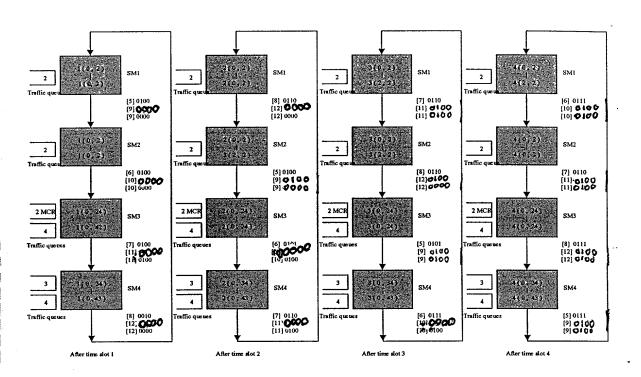


FIGURE 16

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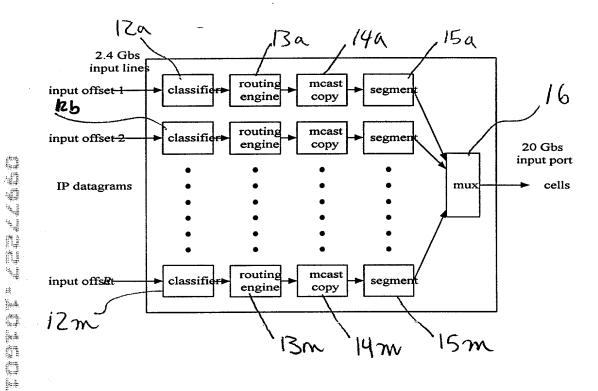


FIGURE 17

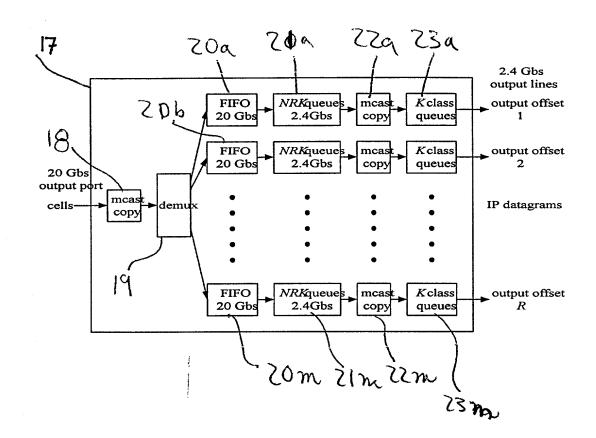


FIGURE 18